

Notice of References Cited	Application/Control No. 09/410,160	Applicant(s)/Patent Under Reexamination BELL ET AL.	
	Examiner Dwin M Craig	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,828,673 A	10-1998	Mikawa et al.	714/718
*	B	US-5,539,652 A	07-1996	Tegethoff, Mauro V.	703/14
*	C	US-6,026,228 A	02-2000	Imai et al.	716/18
*	D	US-6,233,540 B1	05-2001	Schaumont et al.	703/14
*	E	US-6,081,910 A	06-2000	Mifsud et al.	714/718
*	F	US-5,850,348 A	12-1998	Berman, Charles	716/6
*	G	US-5,576,985 A	11-1996	Holtz, Klaus	365/49
*	H	US-6,199,031 B1	03-2001	Challier et al.	703/14
*	I	US-5,970,000 A	10-1999	Kirihata et al.	365/200
*	J	US-6,006,311 A	12-1999	Arimilli et al.	711/133
*	K	US-6,065,134 A	05-2000	Bair et al.	714/7
*	L	US-6,181,614 B1	01-2001	Aipperspach et al.	365/200
*	M	US-5,841,967 A	11-1998	Sample et al.	714/33

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Mark Arnold, Anthony Wallace, Jerry Cupal, John Cowles, "Towards a Formal Model of Hardware Synthesized from Verilog" IEEE 1996, pages 60-66.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.